Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

REMARKS

The foregoing Amendment is filed in response to the official action dated November 17, 2004. Reconsideration is respectfully requested.

The status of the claims is as follows.

Claims 1-8 are currently pending.

Claims 1-8 stand rejected.

Claim 9 has been added.

The Applicants' Attorney wishes to thank the Examiner for affording him the opportunity to clarify the outstanding issues in the above-referenced application during the telephonic interview that took place on March 3, 2005. Before the interview, the Applicants' Attorney provided the Examiner with a Request for Telephonic Interview, including arguments for the patentability of claims 1-8. The interview discussion focused upon these arguments, in view of U.S. Pat. No. 5,951,627 to Kiamilev *et al.*, which is the primary reference cited in the official action. The principal arguments presented to the Examiner during the interview are summarized below.

The Examiner has rejected claims 1-8 under 35 U.S.C. 102(e) as being anticipated by Kiamilev *et al.* Specifically, the

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

official action indicates that the Kiamilev reference discloses a method of computing a fast Fourier transform (FFT) including

(a) receiving N time-ordered first data values;

(b) sequentially storing in a first memory each of said N time-ordered first data values in the time-order;

(c) storing in a second memory a plurality of twiddle factors in a bit reversed order;

(d) reading a predetermined number R of input butterfly data values of said N first data values, wherein said predetermined number R of input butterfly data values are separated by N/R first data values in said N time-ordered first data values;

(e) performing a radix R butterfly calculation on said predetermined number R of input butterfly data values using at least one of the plurality of twiddle factors stored in the second memory to generate R output butterfly data values;

(f) storing said R output butterfly data values in sequential memory locations of a third memory; and

(g) performing said steps (c) - (f) N/R x 2 times, wherein the predetermined number R is the same predetermined number each time the steps (d) - (f) are performed,

wherein said reading step (d) includes reading the R output butterfly data values from said third memory,

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

wherein the memory store operation performed in said storing step (f) has a unity stride, thereby allowing R output butterfly data values to be read from contiguous memory locations each time the R output butterfly data values are read from said third memory, and

wherein said steps (a) – (g) are performed in each one of the plurality of computation stages,

as recited in claim 1. The Applicants respectfully submit, however, that the Kiamilev reference does not disclose each and every step/element of claims 1-8, and therefore the rejections of these claims under Section 102 of the Patent Laws are unwarranted and should be withdrawn.

For example, the Kiamilev reference does not disclose a method of computing an FFT in a plurality of computation stages, as recited in claim 1, including the step of storing R output butterfly data values in *sequential memory locations* of a memory, wherein the memory store operation has *a unity stride*, thereby allowing R output butterfly data values to be read from *contiguous* memory locations *each time* the R output butterfly data values are read from said memory, and wherein *steps (a)-(g) of claim 1 are performed in each one of the plurality of computation stages*. In other words, each one of the computation stages recited in claim 1

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

performs the same processing steps (a)-(g), *i.e.*, the computation stages are substantially identical. Base claims 5 and 8 similarly recite FFT calculation apparatus comprising a plurality of computation stages, in which each computation stage includes the same functional elements, *i.e.*, the computation stages are again substantially identical.

The notion of providing an apparatus and method of computing an FFT in which each stage of the FFT computation performs the same processing steps is described throughout the instant application, *e.g.*, see page 9, lines 1-8, page 12, lines 10-15, and Figs. 3 and 6, of the application. For example, Fig. 3 of the instant application depicts an illustrative FFT calculator stage **300**, which is operative to calculate an 8-point radix-2 FFT (see page 10, lines 8-10, of the application). Further, Fig. 6 of the instant application depicts an illustrative 8-point radix-2 FFT calculation apparatus **600** including three stages **602**, **604**, and **606**. As shown in Fig. 6 of the instant application, each one of the three stages **602**, **604**, and **606** is identical to the FFT calculator stage **300** (see Fig. 3 of the application).

In contrast, the Kiamilev reference discloses a 16-point FFT processor array including stages 1-4, in which each stage provides 16 output butterfly data values (see Fig. 2 of Kiamilev *et al.*).

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

Although stage 4 is depicted as providing its 16 output butterfly data values to sequential locations 0-15, the Applicants respectfully submit that stages 1-3 do not provide their 16 butterfly data value outputs to sequential locations within the FFT processor array. For example, with respect to stage 1, a first butterfly processor having inputs x(0) and x(8) provides its two outputs x(0) and x(1) to non-sequential locations, *i.e.*, a 0^{th} location and a 2^{nd} location, in the FFT processor array; a second butterfly processor having inputs x(1) and x(9) provides its two outputs x(2) and x(3) to non-sequential locations, *i.e.*, a 4^{th} location and a 6^{th} location, in the FFT processor array; a third butterfly processor having inputs x(2) and x(10) provides its two outputs x(4) and x(5) to non-sequential locations, *i.e.*, an 8^{th} location and a 10^{th} location, in the FFT processor array, *etc.* Because the outputs of the butterfly processors in each stage 1-3 of the Kiamilev FFT processor array are not provided to sequential locations like the butterfly processor outputs included in the FFT calculation apparatus **600** (see Fig. 6 of the application), memory store operations at the output of each stage 1-3 of the Kiamilev array would not have a unity stride, as in the method of claim 1.

To assure that the outputs of the butterfly processors in stage 4 are provided to sequential locations in the Kiamilev FFT

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

processor array, a re-shuffling of its outputs x(0)-x(15) is required, as depicted in Fig. 2 of Kiamilev *et al.* This re-shuffling of outputs, which only occurs at the output of stage 4 and does not occur at the outputs of stages 1-3 of the Kiamilev array, is a clear indication that the same processing steps are not being performed in each one of the stages 1-4, as recited in claim 1. Contrary to the assertion in the official action that column 1, lines 55-63, of Kiamilev *et al.* discloses performing the same processing steps in each of the stages 1-4, the Applicants respectfully submit that because of this re-shuffling of the outputs of stage 4, the stages 1-4 of the Kiamilev array do not perform the same processing steps and are therefore not identical.

In addition, the Applicants respectfully point out that the Kiamilev reference discloses a multi-stage FFT calculation system employing multiple virtual memory banks 0-3, in which each bank 0-3 is subdivided into four physical blocks of storage (see Fig. 6 of Kiamilev *et al.*). The Applicants respectfully submit that the output butterfly data values of each stage of the Kiamilev system are not provided to sequential locations of a memory, and therefore the output data values are not read from contiguous memory locations each time the outputs are read from the memory, as recited in claim 1. Instead, output data values are first read

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

from the same address of banks 0 and 2. Next, banks 1 and 3 are accessed at the same address. The accessing of the memory banks 0-3 then alternates between the even-numbered and odd-numbered banks to assure that each butterfly processor gets data inputs that are N/2 points apart from each other (see column 6, lines 15-21, of Kiamilev *et al.*).

In contrast, the method of claim 1 recites the step of storing R output butterfly data values in sequential memory locations of a memory such that the memory store operation has a unity stride, thereby allowing the R output butterfly data values to be read from contiguous memory locations of the memory each time the R output butterfly data values are read from the memory.

This is illustrated in Fig. 6 of the instant application, which depicts the 8-point FFT processor including 3 stages, each stage providing 8 output butterfly data values. Unlike the FFT processor array disclosed in Fig. 2 of the Kiamilev reference, each stage of the FFT processor depicted in Fig. 6 of the application provides its 8 butterfly data outputs to sequential locations within the FFT processor. For example, a first butterfly processor of the first stage of Fig. 6 has inputs x(0) and x(4), and provides its two outputs x(0) and x(1) to sequential locations, *i.e.*, a 0^{th} location and a 1^{st} location, in the FFT

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

processor. Similarly, a second butterfly processor of the first stage having inputs x(1) and x(5) provides its two outputs x(2) and x(3) to sequential locations, *i.e.*, a 2nd location and a 3rd location, in the FFT processor. The remaining butterfly processors of the first stage also provide their outputs to sequential locations 4-7 in the FFT processor, as do the butterfly processors contained in each one of the second and third stages of the FFT processor.

Significantly, no alternating between even-numbered and odd-numbered memory banks, as taught by Kiamilev *et al.*, is required in the method of claim 1 to assure that each butterfly processor receives data inputs that are N/2 points apart from each other. As a result, the method of claim 1 can be used to compute an FFT in a manner that both reduces the number of required iterations and simplifies the calculation of the storage locations of the output data values from each memory stage (see page 6, lines 17-21, of the application). Clearly, a data storage scheme that requires alternating between even-numbered and odd-numbered memory banks to assure that each butterfly processor in a respective computation stage receives data inputs that are N/2 points apart from each other, as taught in the Kiamilev reference, does not

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

achieve the disclosed advantage of simplifying the calculation of the storage locations of the output data values.

Because the Kiamilev reference neither teaches nor suggests that R output butterfly data values are stored in sequential memory locations of a memory such that the memory store operation (step (f) of claim 1) has a unity stride, thereby allowing the R output data values to be read from contiguous memory locations of the memory each time the R output data values are read from the memory, and that steps (a) - (g) of claim 1 are performed in each one of the FFT computation stages, as recited in claim 1, the Kiamilev reference does not anticipate claim 1. Moreover, because limitations equivalent to those indicated above are also included in base claims 5 and 8, the Kiamilev reference does not anticipate claims 5 and 8. Accordingly, it is respectfully submitted that the rejections of claims 1, 5, and 8 and the claims dependent therefrom under section 102 of the Patent Laws are unwarranted and should be withdrawn.

As indicated above, base claim 9 has been added to more distinctly claim an embodiment of the Applicants' FFT computation method. Like claims 1, 5, and 8, added claim 9 recites a plurality of stages for computing the FFT, in which each stage performs the same processing steps (a)-(g), *i.e.*, the computation

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

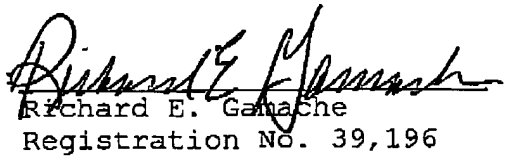
stages are substantially identical. Because none of the art of record discloses or suggests a method or apparatus as claimed, in which all computation stages are substantially identical, and in which each stage stores output butterfly data values in sequential locations of a memory, it is believed that claim 9 is allowable over the art of record.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

MARC HOFFMAN, ET AL.

By 
Richard E. Gamache
Registration No. 39,196
Attorney for Applicants

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
Ten Post Office Square
Boston, MA 02109
Telephone: (617) 542-2290
Telecopier: (617) 451-0313

REG/pjd
Enclosure
318200